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# (54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To maintain impurities on retrograde by implanting ions of the same conductivity type as that of a substrate into the inside of the substrate after formation of a gate oxide film and a gate, and performing channel doping, and performing annealing for activation limitedly at low temperature and in a short time.

CONSTITUTION: A polysilicon film 4 is grown as an electrode film all over the surface of a substrate. A high-concentration p-type layer 5 is formed by implanting B+ ions into the surface of the polysilicon substrate 1. The polysilicon film 4 is patterned into a gate, and with the gate as a mask, a source 6 and a drain 7 are formed by implanting As+ ions, and also the gate is doped with arsenic. A PSG film 8 is grown as a layer insulating film on the substrate. Next, by the RTA by lamp heating, the heat treatment at 900°C and in a short time of 20 sec is performed on the substrate. In this case, since the heat treatment time is very short, the impurities having ions implanted are electrically activated, but rediffusion hardly occurs.

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## CLAIMS

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[Claim(s)]

[Claim 1] Form gate dielectric film 3 on the 1 conductivity-type semi-conductor substrate 1, and with this first process that puts the gate electrode layer 4 all over a gate-dielectric-film top subsequently With the second process which pours in 1 conductivity-type impurity ion with energy with which average projection range exists in the interior of this semi-conductor substrate through this gate electrode layer and this gate dielectric film, subsequently The manufacture approach of the semiconductor device which distribution of the depth direction of this 1 conductivity-type impurity has the maximal value inside this semi-conductor substrate, and is characterized by having the temperature chosen so that it might be maintained that it is low concentration, and the third process which heat-treats this semi-conductor substrate by time amount from this on this semi-conductor substrate front face.

[Claim 2] The manufacture approach of the semiconductor device according to claim 1 characterized by having the process which puts the 2nd gate electrode layer all over a gate electrode layer top after said second process.

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DETAILED DESCRIPTION

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[Detailed Description of the Invention]

[0001]

[Industrial Application] The manufacture approach of a semiconductor device is started and this invention is especially MOS FET. It is related with the manufacture approach.

Recent years and MOS FET Although it is made detailed and channel length is becoming short, in connection with this, FET does not carry out a punch-through breakdown, It is required that it should have quantity current driving force.

[0002]

[Description of the Prior Art] Former, A semiconductor device is reducing the dimension of the component carried in it, Improvement in the speed and high integration have been advanced. However, the component to carry is MOS FET. If channel length is reduced to a case The so-called short channel effects, such as a fall of the threshold electrical potential difference Vth and a fall of punch-through breakdown voltage, occur, This had become the failure which obstructs detailed-ization of a semiconductor device.,

[0003] short channel effect, While channel length becomes short the rate of the field which the depletion layer prolonged from the source drain to the whole channel field occupies -- increasing -- potential -- the gate -- not but It is generated by mainly coming to rule over with a drain.

[0004] Therefore, when you are going to make it reduce channel length, controlling this short channel effect, it is, He makes the high impurity concentration of a substrate, i.e., a channel field, increase, and is trying to suppress stretch of the depletion layer from a source drain small. In that case It is usually channel length's dimension reduction percentage and EQC, or -1/2. If gate dielectric film is thin-film-ized by the ratio of **** Without it raises a threshold electrical potential difference A short channel effect can also be controlled.,

[0005] However, when the impurity of a channel field is made to increase uniformly, it is, The perpendicular electric field impressed to the carrier in a channel increase. Therefore, the mobility of a carrier falls, and a current does not increase to the forge fire which reduces a dimension, but improvement in the speed becomes is hard to be promoted.

[0006] moreover Request which controls the fall of the dependability by a hot carrier effect etc. Channel length 0.5-0.6 From the device which is mum grade 5 V of the former [ supply voltage / VDD ] 3.3 V It has come to be reduced by extent. To this sake Active region more than a threshold electrical potential difference, Namely, in order to take large VDD-Vth and to secure current driving force A value also with a still lower threshold electrical potential difference comes to be required, and this inclination continues, as long as detailed-ization of a device progresses.,

[0007] as mentioned above In order to solve the trouble at the time of making the impurity of a channel field increase uniformly and reducing a device Concentration

distribution of retro grade, namely, the impurity distribution which made height concentration near [ as junction of the source drain which is easy to produce a punch-through / same ] the depth -- forming -- a short channel effect -- controlling -- and He is trying to keep the mobility of a carrier high., FET of such [ drawing 2 ] punch-through suppression structure A sectional view is shown.

[0008] For a p type semiconductor substrate and 2, as for gate oxide and 4, in drawing 2 , field oxide and 3 are [ 1 / the gate and 5 ] high concentration p type layers. With this structure, the high concentration p type layer 5 is formed in the channel field bottom.

[0009]

[Problem(s) to be Solved by the Invention] However, in the manufacture approach which is generally performed and which carries out a channel dope by the ion implantation, and forms gate dielectric film after that, even if it forms concentration distribution of retro grade, since the oxidation process of gate-dielectric-film formation is generally an elevated temperature, the impurity distribution immediately after impregnation will collapse by thermal diffusion, and will turn into uniform concentration distribution.

[0010] Drawing 3 is drawing explaining signs that impurity distribution of the depth direction of a channel field changes with gate oxidization. drawing -- (1) Immediately after impregnation and (2) Concentration pro FAIRU after gate oxidation is shown.

[0011] Here, it is mainly based on a request from dependability that gate oxidation is an elevated temperature. This is an n-channel MOS FET which uses boron with a large diffusion coefficient for a channel dope. It sets and is a p channel MOS. FET It is a serious problem.

[0012] Furthermore, when using the partial pressure oxidation style which dilutes oxygen with inert gas to gate oxidation, and oxidizes from the usual thermal oxidation at an elevated temperature to it, it is much more serious. Since insulation is excellent even if it thin-film-izes, the oxide film formed with this partial pressure oxidation style is MOS FET. In detailed-izing, it is becoming an important technique.

[0013] This invention, Even if an elevated-temperature gate acid chemically-modified degree is contained The manufacture process which saves a channel profile with impurity distribution of retro grade is offered, and it is MOS FET. A short channel effect is controlled, It aims at contributing to detailed-ization of a semiconductor device.,

[0014]

[Means for Solving the Problem] Solution of the above-mentioned technical problem forms gate dielectric film 3 on 1 1 conductivity-type semi-conductor substrate 1, and with this first process that puts the gate electrode layer 4 all over a gate-dielectric-film

top subsequently With the second process which pours in 1 conductivity-type impurity ion with energy with which average projection range exists in the interior of this semi-conductor substrate through this gate electrode layer and this gate dielectric film, subsequently So that distribution of the depth direction of this 1 conductivity-type impurity may have the maximal value inside this semi-conductor substrate and it may be maintained from this on this semi-conductor substrate front face that it is low concentration the manufacture approach of a semiconductor device of having the selected temperature and the third process which heat-treats this semi-conductor substrate by time amount, or 2 -- it is attained by the manufacture approach of the semiconductor device said one publication of having the process which puts the 2nd gate electrode layer all over a gate electrode layer top after said second process.

[0015]

[Function] With this invention After forming gate oxide and the gate The ion of a substrate and this conductivity type is poured in with energy which has average projection range in the interior of a substrate, a channel dope is performed, and activation annealing of the impurity after an ion implantation is limited to low temperature and a short time, and is performed, He is trying to maintain impurity distribution of retro grade.,

[0016] Therefore, the impurity in the deep place for functioning as a punch-through stopper by which the ion implantation was carried out does not carry out redistribution.

[0017]

[Example] Drawing 1 (A) - (D) It is a sectional view explaining the example of this invention. Drawing 1 (A) It sets and is selective oxidation (LOCOS). By law, it considers as the field oxide which carries out demarcation expression of the component formation field, and the diacid-ized silicon (SiO2) film 2 is formed in the silicon (Si) substrate 1.

[0018] It ranks second, For example, A substrate is oxidized thermally in the desiccation oxygen ambient atmosphere of 850 ** Thickness 5 nm SiO2 film 3 is formed as gate oxide. Subsequently, vapor growth (CVD) By law, the polish recon film 4 with a thickness of 100nm is grown up as a gate electrode layer all over a substrate top.

[0019] Drawing 1 (B) It sets and is boron ion (B+) from a substrate front face. Energy It pours in on condition that 60 KeV and dose 5E12cm-2, and the high concentration p type layer 5 is formed. If an ion implantation is performed on this condition The high concentration p type layer 5 is about 0.1 from a substrate front face. It has a peak at the place of mum, It becomes low concentration toward a front face at ****.,

[0020] Drawing 1 (C) It sets, and patterning of the polish recon film 4 is carried out, it considers as the gate, the gate is used as a mask, and it is arsenic ion. (As+) Energy It pours in on condition that 20 KeV and dose 4E15cm-2, and while forming the source 6 and a drain 7, arsenic is doped also to the gate.

[0021] Drawing 1 (D) It sets and is CVD. Silica glass which does not get thickness 300 nm as an interlayer insulation film on a substrate by law (PSG) The film 8 is grown up. subsequently Rapid thermal annealing (RTA) by lamp heating etc. ****** Substrate 900 degrees C and a short time for 20 seconds are heat-treated. In this case Although the impurity by which the ion implantation was carried out is electrically activated since heat treatment time amount is very short Re-diffusion hardly takes place.,

[0022] Subsequently, PSG A contact hole 9 is formed in the film 8, the aluminum (aluminum) wiring 10 is formed, and it is at the last, It is Covering PSG as a protective coat on it. The film 11 is put and it completes. Although this example explained the case where the gate electrode layer 4 was deposited at 1 time of a process, the gate electrode layer 4 is divided [ steeper pro FAIRU or ] into two times to form more deeply, and the high concentration p type layer 5 is deposited. The example in this case is shown below.

[0023] Gate oxide 3 is formed like the above-mentioned example, and it is thickness about the 1st layer gate electrode layer. It deposits in 20nm and is energy about boron ion. It pours in on condition that 35 KeV and dose 5E12cm-2, and the high concentration p type layer 5 is formed. It ranks second, It is thickness about a two-layer eye gate electrode layer. It deposits in 20 nm and is sum total thickness. 100 nm The gate is formed.

[0024] In this case Compared with the case where a gate electrode layer is formed at once, since it can form in the same depth with low energy, breadth is stopped small and the high concentration p type layer 5 serves as steep impurity distribution.

[0025] Although the above example explained the case where an n channel component was formed in p mold substrate, this invention can completely be similarly applied, when forming a p channel component.

[0026]

[Effect of the Invention] According to this invention Even if an elevated-temperature gate acid chemically-modified degree is contained The manufacture process which saves a channel profile with impurity distribution of retro grade is offered, and it is MOS FET. A short channel effect is controlled, It aims at contributing to detailed-ization of a semiconductor device.,

## DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The sectional view explaining the example of this invention

[Drawing 2] FET of punch-through suppression structure Sectional view

[Drawing 3] Drawing explaining signs that impurity distribution of the depth direction of a channel field changes with gate oxidization

[Description of Notations]

1 It is Semi-conductor Substrate and is Si Substrate.

2 It is Field Oxide and is SiO2 Film.

3 It is Gate Oxide and is SiO2 Film.

4 It is Gate Electrode Layer and is Polish Recon Film.

5 High Concentration P Type Layer

6 Source

7 Drain

8 It is Interlayer Insulation Film and PSG. Film

9 Contact Hole

10 Aluminum-Wire with Metal Wiring.

11 Covering PSG Film